module srlatchtb;

reg clk;

reg s, r;

wire q, qb;

srlatch uut(.s(s), . r(r), .q(q), .qb(qb));

initial begin

clk = 0;

forever #5 clk = ~clk;

end

initial begin

$dumpfile("srlatch.vcd");

$dumpvars(1);

end

initial begin

clk = 0;

s = 0;

r = 0;

end

always @(posedge clk) begin

s = 1;

r = 0;

#10;

s = 0;

r = 1;

#10;

s = 1;

r = 0;

#10;

s = 0;

r = 1;

#10;

s = 1;

r = 0;

#5;

s = 0;

r = 0;

#10;

s = 0;

r = 1;

#5;

s = 0;

r = 0;

#10;

$finish;

end

endmodule

module srlatch(s,r, q,qb);

input s,r;

output q,qb;

wire nand1, nand2;

nand (nand1, s, qb);

nand (nand2, r, q);

nand (q, nand1, q);

nand (qb, nand2, qb);

endmodule